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EXAMINER	
SAVLA, ARPAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,964	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 31, 2007 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed October 31, 2007 in response to the Office action dated July 10, 2007. Claims 21 and 35-43 have been amended. Claims 21-52 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendments, the objection to the specification has been withdrawn.

Claims

2. **Claim 21** is objected to because of the following informalities:

On lines 5-6 the term "at least one host computer**s**" should instead read "at least one host computer."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 21-28 and 30-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis et al. (U.S. Patent 6,343,324) in view of Katzman et al. (U.S. Patent 4,228,496) (hereinafter "Katzman").

5. **As per claim 21**, Hubis discloses a storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said disk drives (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data, which are sent from at least one host computer to said logical volume for updating said logical volume, in said disk drives (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180); *It should be noted that the "Processor 180" is analogous to the "processor adapter."*

a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least

one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1 – 184-M); *It should be noted that the "I/O Processors 184-1-M" are analogous to the "plurality of first interface adapters."*

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186); *It should be noted that the "Data Cache Memory" is analogous to the "memory adapter."*

a plurality of second interface adapters each receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said at least one processor adapter and storing data received at each of said second interface adapters in said disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processors 185-1-M" are analogous to the "plurality of second interface adapters."*

a switch adapter coupled to said processor adapters, said first interface adapters, said memory adapter and said second interface adapters and relaying data between said first interface adapters and said memory adapter and relaying data between said memory adapter and said second interface adapters (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that the "PCI Bus Interface and Memory Controller" is analogous to the "switch adapter."*

wherein said switch adapter relays said first and said second control information between said processor adapters and said first interface adapters and relays said third control information between said processor adapters and said second interface adapters (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not expressly disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased based on a required performance.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33); *It should be noted that the "processor modules" are analogous to the "processor adapters."*

wherein the number of said processor adapters are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no

change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 21.

6. **As per claim 22**, the combination of Hubis/Katzman discloses said processor adapters are independently attached to or detached from said first interface adapters (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41). *It should noted that the "device controllers" are analogous to the "interface adapters."*

7. **As per claim 23**, the combination of Hubis/Katzman discloses said processor adapters are assigned to a process of at least one said first interface adapter and a process of at least one said second interface adapter (Hubis, col. 16, lines 6-9).

8. **As per claim 24**, the combination of Hubis/Katzman discloses said at least one processor adapter is assigned to said plurality of first interface adapters (Hubis, col. 16, lines 6-9).

9. **As per claim 25**, the combination of Hubis/Katzman discloses said at least one processor adapter is assigned to said plurality of second interface adapters (Hubis, col. 16, lines 6-9).

10. **As per claim 26**, the combination of Hubis/Katzman discloses it is possible to increase or decrease the number of said processor adapters in case that the number of

said first interface adapters is not increased or decreased (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

11. **As per claim 27**, the combination of Hubis/Katzman discloses it is possible to change the number of said processor adapters on storing data in said disk drives (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33).

12. **As per claim 28**, the combination of Hubis/Katzman discloses the number of said processor adapters is increased or decreased in accordance with the number of said first interface adapters being increased or decreased (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

13. **As per claim 30**, the combination of Hubis/Katzman discloses said first control information is used to notify said at least one processor adapter of receiving said write request (Hubis, col. 15, lines 10-25).

14. **As per claim 31**, the combination of Hubis/Katzman discloses said at least one processor adapter detects an area of said memory in which data of said logical volume need to be stored in accordance with said received first control information (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). *It should be noted that it is inherently required Processor 180 detect/recognize an area of the Data Cache Memory in order to allocate space for storing data in the Cache Memory during a write task.*

15. **As per claim 32**, the combination of Hubis/Katzman discloses said second control information includes information related to an area of said memory in which data received at said first interface adapter need to be stored (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). I*t should be noted that it is inherently required Processor*

180 allocate/reserve an area of the Data Cache Memory in order to store data in the Cache Memory during a write task.

16. **As per claim 33**, the combination of Hubis/Katzman discloses said at least one processor adapter finds an area of said disk drives related to said logical volume for storing data of said logical volume based on said received first control information (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

17. **As per claim 34**, the combination of Hubis/Katzman discloses said third control information includes information related to an area of said disk drives in which data received at said second interface adapter need to be stored (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

18. **As per claim 35**, the combination of Hubis/Katzman discloses said at least one processor adapter controls to create a parity data of RAID (Redundant Array of Inexpensive Disks) from data received at least one of said first interface adapters (Hubis, col. 4, line 64 – col. 5, line 3).

19. **As per claim 36**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from

said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1); *It should be noted that the "I/O Processor 184-1" is analogous to the "first interface adapter."*

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processor 185-1" is analogous to the "second interface adapter."*

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter and relaying said data among said first interface adapter, said memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays said first and said second control information between said processor adapter and said first interface adapter and relays said third control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not expressly disclose the number of said processor are increased or decreased, if the number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased.

Katzman discloses the number of said processor are increased or decreased, if the number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a

multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 36.

20. **As per claim 37**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a second control information sent from said processor

adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter and relaying data of said logical volume among said first interface adapter, said memory adapter and said second interface adapter and not relaying data of said logical volume to said processor adapter (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that when the host sends a read request to the logical volumes, Processor 180 does not receive the read data itself, but rather controls the process of sending the read data back to the host.*

wherein said switch adapter relays said first control information between said processor adapter and said first interface adapter and relays said second control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not expressly disclose it is possible to change the number of said processor adapter on storing on storing data in said disk drives.

Katzman discloses it is possible to change the number of said processor adapter on storing on storing data in said disk drives (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 37:

21. **As per claim 38**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said first interface adapter, said processor adapter, and said memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays data between said first interface adapter and said second interface adapter via said memory adapter among said first interface adapter, said processor adapter, said memory adapter and said second interface adapter based on control information transferred among said first interface adapter, said processor adapter and said second interface adapter of said first interface adapter, said processor adapter, said memory adapter, and said second interface adapter (col. 15, lines 63-66; col. 15, line 67 – col. 16, line; Fig. 2A, elements 183 and 186). *It should be noted that Data Cache Memory buffers any data sent between I/O Processor 184-1 and I/O Processor 185-1.*

Hubis does not expressly disclose the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased.

Katzman discloses the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 38.

22. **As per claim 39**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from

said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and sends said second control information to said first interface adapter and sends said third control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends data to said memory adapter among said processor adapter, said memory adapter and said second interface adapter (col. 15, line 67 – col. 16, line 3);

wherein said second interface adapter receives data from said memory adapter among said processor adapter, said memory adapter and said first interface adapter (col. 16, lines 3-6);

wherein said memory adapter receives data from said first interface adapter and said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 15, line 67 – col. 16, line 6);

Hubis does not expressly disclose the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased based on a required performance.

Katzman discloses the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 39.

23. **As per claim 40**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said disk drives (col. 7, lines 27-28; Fig. 2, element 108);

at least one processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drives (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

at least one first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

at least one a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and sends said first control information to said first interface adapter and sends said second control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends data of said logical device volume to said memory adapter among said processor adapter, said memory adapter and said second interface adapter (col. 15, lines 19-22; col. 15, line 67 – col. 16, line 3); *It should be noted that when a write request is received, data to be written into the logical device is buffered in the Data Cache Memory.*

wherein said second interface adapter receives data of said logical volume from said memory adapter among said processor adapter, said memory adapter and said first interface adapter (col. 15, lines 19-22; col. 16, lines 3-6); *It should be noted that when a read request is received, data read from the logical device is buffered in the Data Cache Memory.*

wherein said memory adapter receives data of said logical volume from said first interface adapter and said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 15, line 67 – col. 16, line 6).

Hubis does not expressly disclose the number of said processor adapter is increased or decreased in accordance with the number of said first interface adapter is increased or decreased.

Katzman discloses the number of said processor adapter is increased or decreased in accordance with the number of said first interface adapter is increased or decreased (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 40.

24. **As per claim 41**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from

said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and sends said first control information to said first interface adapter and sends said second control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends said data received at said first interface adapter to said memory adapter and does not send said data received at said first interface adapter to said processor adapter (col. 15, line 67 – col. 16, line 3); *It should be noted that when the host sends a write request to the logical volumes, Processor*

180 does not receive the write data itself, but rather controls the process of sending the write data to the logical volume.

wherein said second interface adapter receives said data stored in said memory adapter from said memory adapter and does not receive said data stored in said memory adapter from said processor adapter (col. 16, lines 3-6); *It should be noted that when the host sends a write request to the logical volumes, Processor 180 does not receive the write data itself, but rather controls the process of sending the write data to the logical volume. Therefore, the data sent to I/O Processor 185-1 from the Data Cache Memory is not from the Processor 180.*

wherein said memory adapter receives said data sent from said first interface adapter and does not receive data from said processor adapter (col. 15, line 67 – col. 16, line 3); *See the citation note for the limitation directly above.*

Hubis does not expressly disclose the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased.

Katzman discloses the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage

system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 41.

25. **As per claim 42**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to read data by determining a location at which the data should be read, the data being related to a read request sent from said host computer to said logical volume for reading data of said logical volume, from said disk drive (col. 15, lines 19-25; col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving said read request and sending a first control information related to said read request to said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a second interface adapter receiving data stored in said disk drive from said disk drive based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

a memory adapter having at least one memory, said memory storing data sent from said second interface adapter; (col. 16, lines 3-6; Fig. 2A, element 186);

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter and relaying data received at said second interface adapter between said second interface adapter and said memory adapter and relays said first control information between said first interface adapter and said processor adapter and relays said second control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

wherein said first interface adapter receives data stored in said memory adapter from said memory adapter based on a third control information sent from said processor adapter and sends data received at said first interface adapter to said host computer (col. 15, line 67 – col. 16, line 3);

wherein said switch adapter relays data stored in said memory adapter between said memory adapter and said first interface adapter and relays said third control information between said processor adapter and said first interface adapter (col. 15,

lines 63-66; Fig. 2A, element 183); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not expressly disclose the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased based on a required performance.

Katzman discloses the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 42.

26. **As per claim 43**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to read data data by determining a location at which the data should be read, the data being related to a read request sent from said host computer to said logical volume for reading data of said logical volume, from said disk drive (col. 15, lines 19-25; col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving said read request and sending a first control information related to said read request to said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a second interface adapter receiving data stored in said disk drive from said disk drive based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

said memory adapter having at least one memory, said memory storing data sent from said second interface adapter; (col. 16, lines 3-6; Fig. 2A, element 186);

wherein said first interface adapter receives data stored in said memory adapter and sends data received at said first interface adapter to said host computer based on a

third control information sent from said processor adapter (col. 15, line 67 – col. 16, lines 9);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and receives said first control information from said first interface adapter and sends said second control information to said second interface adapter and sends said third control information to said first interface adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 6);

wherein said first interface adapter receives data from said memory adapter among said processor adapter, said memory adapter and said second interface adapter (col. 15, line 67 – col. 16, line 3);

wherein said second interface adapter sends data to said memory adapter among said processor adapter, said memory adapter and said first interface adapter (col. 16, lines 3-6);

wherein said memory adapter receives data from said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 16, lines 3-6);

Hubis does not expressly disclose wherein the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased, if the number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased.

Katzman discloses wherein the number of a plurality of processor adapters, which each correspond to said processor adapter, are increased or decreased, if the

number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased (col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

Therefore, it would have been obvious to combine Hubis and Katzman for the benefit of obtaining the invention as specified in claim 43.

27. **As per claims 44-52**, the combination of Hubis/Katzman discloses the memory adapter includes a control information memory module in which information for controlling data transfer is stored (Hubis, col. 15, line 67 – col. 16, line 3; col. 8, lines 2-5; Fig. 2A, element 186).

28. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Katzman, as applied to claim 21 above, and further in view of Kuchta et al. (U.S. Patent 6,014,319) (hereinafter "Kuchta").

29. **As per claim 29**, the combination of Hubis/Katzman does not expressly disclose a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters;

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters;

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter.

Kutcha discloses a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters (col. 7, lines 15-18; Fig. 2A, element 245; Fig. 2B, elements 211-212); *It should be noted that "I/O modules 211-212" are analogous to the "first portion of processor adapters" and "I/O cards 245" are analogous to "first interface adapters."*

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters (col. 7, lines 35-38; Fig. 2A, element 246; Fig. 2B, elements 209-210); *It should be noted that "I/O modules 209-210" are analogous to the "second portion of processor adapters" and "I/O cards 246" are analogous to "second interface adapters."*

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter (col. 5, lines 59-63). *It should be noted that amount of I/O modules 209-210 versus the amount of*

I/O modules 211-212 (i.e. a proportion between said first portion and said second portion) is based on performance characteristics.

The combination of Hubis/Katzman and Kuchta are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Kuchta's additional I/O modules within Hubis/Katzman's storage system.

The motivation for doing so would have been to provide later system enhancements (Kuchta, col. 5, lines 49-50).

Therefore, it would have been obvious to combine Hubis/Katzman and Kuchta for the benefit of obtaining the invention as specified in claim 29.

Response to Arguments

30. Applicant's arguments filed October 31, 2007 with respect to **claims 21-52** have been fully considered but they are not persuasive.

31. With respect to Applicant's argument in the first and third full paragraphs on page 24 of the communication filed October 31, 2007, upon further consideration, the Examiner respectfully disagrees. In Hubis, when a host computer 101-M attempts to write to or read from a logical volume 108-M, array controller 106 completes the host-to-volume mapping for the write or read operation. This whole process is completed using the NVRAM data structures 182. Port mapping table 190 is used to configure logical volumes 180-N to host computers 101-M so as to determine where data should be

written to or read from in the logical volume based on the host computers write or read command. Operations within the NVRAM data structures 182 including port mapping table 180 are all controlled by Processor 180 which coordinates the activities of all of the I/O processors 184-185. Thus, overall it is Processor 180 that determines a location at which the data should be stored or read based on the host-to-volume mapping. Accordingly, Hubis' Processor 180 sufficiently discloses Applicant's process adaptor.

32. With respect to Applicant's argument in the first full paragraph on page 25 of the communication filed October 31, 2007, the argument has been considered but is moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 21-52** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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